Remarks

Claims 1-94 are pending for consideration. Claims 1, 12, 23, 31, 39, 45, 53, 55-56 70, and 87 have been amended. In view of the above amendments and following remarks, Applicant respectfully requests reconsideration and allowance of the subject application.

Statement of Substance of Interview Dated 4/9/ 2007

Applicant wishes to thank Examiner Nadia Khoshnoodi for conducting a informal telephonic interview with Applicant's attorney, Daniel T. McGinnity, on 4/9/2007., regarding the Advisory Action dated 4/5/07. During the interview, Examiner Khoshnoodi confirmed that an Advisory Action had been mailed. Further, Examiner Khoshnoodi offered clarifications regarding remarks made in the Advisory Action. In particular amendments directed at subject matter on p. 26-27 of the subject application referenced in the Advisory Action were discussed. Applicant understood the Examiner as tenatively agreeing that clarifications to the recited "per cache page basis" would overcome the art of record. Accordingly, in the interest of expediting allowance of the subject application, and without conceding the propriety of the rejections, each of the independent claims is amended herein to incorporate subject matter discussed during the interview.

§ 102 and § 103 Rejections

Claims 23, 26-27, 30-31, 34-35, 38-39, 41 and 44 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent Application Publication No. 2005/0102264 ("Nason").

Claims 1-2, 5-8, 11-13, 16-20, 40, 42, 45, 48-50 and 52 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Nason, in view of U.S. Patent Application Publication No. 2002/0136408 ("Garcia").

Claims 3-4, 14-15 and 46-47 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Nason in view of Garcia, in further view of U.S. Patent No. 5,727,062 ("Ritter").

Claims 9-10 and 20-21 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Nason in view of Garcia, in further view of U.S. Patent No. 5,572,235 ("Mical").

Claims 24-25, 32-33 and 43 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Nason in view of Ritter.

Claims 28-29 and 36-37 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Nason in view of Mical.

Claim 51 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Nason in view of Garcia, in further view of U.S. Patent No. 6,934,389 ("Strasser").

Claims 53-56, 59, 63-66, 69-73, 76, 80-83 and 86 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Nason in view of Strasser.

Claims 87, 89-92 and 93-94 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Nason in view of Garcia, in further view of Strasser.

Claims 57-58, 74-75 and 88 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Nason in view of Strasser, in further view of Ritter.

Claims 60-62 and 77-79 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Nason in view of Strasser, in further view of Garcia.

Claims 60-62 and 77-79 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Nason in view of Strasser, in further view of Garcia.

Claims 67-68 and 84-85 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Nason in view of Strasser, in further view of Mical.

Applicant maintains that the Office has not established a *prima facie* case of anticipation or obviousness with respect to the pending claims for at least the reasons discussed in previous Response dated 2/7/07. In the Response dated 2/7/07, Applicant submitted patentability arguments with respect to the cited references including that:

- The references of record fail to disclose, teach, or suggest "at least one of said acts of decrypting and re-encrypting taking place on a per cache page basis" as recited for example in claim 1.
- The references of record fail to disclose, teach, or suggest "a cryptographic processor that resides on the video card" as recited for example in claim 1.
- The Garcia reference is non-enabling with respect to "a cryptographic processor that resides on the video card" for which it is relied upon.
- The references teach away from the proposed combination.
- The proposed combination lacks motivation at least because it would change the principle of operation of the Nason reference.

The previous Response and arguments made therein are maintained and hereby incorporated by reference. Nonetheless, in the interest of expediting allowance of the

subject application, and without conceding the propriety of the rejections, each of the independent claims is amended herein to clarify the recited "per cache basis" as was suggested by the Examiner and discussed in the interview of 4/9/2007. In particular, the claims have been amended to clarify that per cache page basis operations are performed by the GPU utilizing encryption/decryption hardware of the GPU. Support for the amendments may be found through the specification and drawings as filed, examples of which include p. 21-23; FIG. 6; and p. 25-27. For example:

Claim 1 as amended recites in part a method comprising:

- at least one of said acts of decrypting and re-encrypting taking place on a per cache page basis ***and being performed by encryption/decryption hardware integrated with the GPU***. (emphasis added)

The proposed combinations of references fails to disclose, teach, or suggest any such features. Nason is relied upon in each of the proposed combinations for the recited feature of "per cache basis". For reasons submitted in the previous response dated 2/7/07, Applicant maintains that Nason does not in fact describe this positively recited feature of the claims. Further, Nason describes techniques performed by a security-enhanced driver (SEDD), which is consistently and clearly described as software residing between the operating system and hardware. The SEDD is software executed via a microprocessor (CPU) away from the video card and/or GPU. Thus, Nason describes techniques which are not equivalent to the recited features of claim 1. Further, the SEDD techniques described in Nason are not compatible with and teach away from the claimed features.

In rejecting claim 1, Nason at paragraph [0056], which describes FIG. 7, is relied upon for "at least one of said acts of decrypting and re-encrypting taking place on a per cache page basis" as recited in claim 1. Applicant respectfully disagrees. Nason is completely devoid of any teachings or suggestion related to an act of "decrypting or re-encrypting on a per cache page basis". For example, Nason makes no mention whatsoever of a "cache page", "cache", or any of their respective equivalents. More to the point, Nason expresses no concern at all for any cache (of a GPU or otherwise) or any operations performed in such a context. Paragraph [0056] of Nason addresses moving portions of a frame in VRAM and masking a portion with an already obfuscated portion. This apparently occurs outside of any obfuscation/deobfuscation. Thus, Nason in the cited portion teaches measures that are performed with respect to secure **portions** of information, eventually resident in VRAM, under the control of an SEDD. Nasson lacks disclosure indicating that decrypting or re-encrypting, assuming this occurs, is performed on a per cache page basis. For instance, Nason is silent on how or if element 708 of FIG. 7 (obfuscated data) is decrypted or re-encrypted. There is no basis for a conclusion that the obfuscation occurs on a per cache page basis outside of the applicant's own disclosure and claims. Simply rearranging portions of data in memory as in FIG. 7 and paragraph [0056] of Nason is not equivalent to the claimed feature. For at least these reasons, Nason does not teach or suggest the "per cache page basis" aspect for which it is cited.

Even if Nason is somehow construed as providing the claimed aspect of "per cache page basis" (which applicant maintains it does not), Nason still lacks "acts . . . taking place on a per cache page basis and being performed by encryption/decryption

hardware integrated with the GPU" (emphasis added) as presently recited in claim 1. Nason contemplates **only** those security measures that are implemented by way of conventional, widely-known video card technology under the control of a security-enhanced driver (SEDD), and that such is fundamental to the principle of operation of the Nason teachings. That is, the SEDD of Nason operates by way of a corresponding microprocessor of the client computer from a location **off** the video card. Thus, the Applicant further contends, any encrypted or decrypted data under Nason is derived by way of microprocessor operations separate and apart from any video card. Accordingly, Nason lacks any basis for "decrypting and re-encrypting taking place on a per cache page basis and being performed by encryption/decryption hardware integrated with the GPU".

Nason does describes methods and systems for preventing the unauthorized access, interception and/or modification of computer code on a client device and, among other things, such data as pertaining to graphical information resident in VRAM of a video card (Abstract, *et seq.* of Nason). However, it is important to note that under **every** procedure or method taught by Nason - pertinent in any way to information resident on a video card - the Security Enhanced Display Driver (SEDD) plays an essential role in the "scheduling" (i.e., control, derivation, provision and/or exchange) of secured data. For example, Nason recites:

> "In one embodiment, **a security enhanced display driver (SEDD)** is provided to schedule content of portions of a frame buffer stored in a video display memory. In one such embodiment, a request to display data to a secure region on a video display made to **the SEDD**. In response, **the SEDD allocates** a corresponding secure portion of the frame buffer and **schedules** the data content of this secure portion such that valid data is only present in the secure portion at the time it is needed for projection to the display device and when other tasks are locked out of accessing (reading or writing) to the secure portion. The SEDD **determines**, depending upon, the obfuscation techniques used, when data stored in the secure portion needs to be de-obfuscated and when it needs to be re-obfuscated. *Nason, paragraph [0011].*

Nason in another passage indicates:

> the security enhanced drivers (SEDs) 406 preferably reside between the operating system device drivers 405 and the hardware so as to better control secure processing of input and output in the lowest layers of a computing system. *Nason, paragraph [0043].*

Thus, Nason groups the SEDD together within all other drivers, software and the operating system used by the client computer to be kept secure (Fig. 1 of Nason). Nason further makes it clear that the operating system, display driver (i.e., SEDD), and other software reside and are utilized by a processor **away from** both the video card and any VRAM resident thereon (Figs. 2 and 4 of Nason). Thus Nason is not compatible with the claimed features which involve hardware of the GPU. Nason is limited to obfuscation/deobfuscation performed by the SEDD software situated between the OS and Hardware, e.g., not the hardware, video card or GPU itself. Thus, it is impossible for Nason to provide the features of claim 1 for which it is relied upon.

Simply put, Nason is directed a providing a different result in a different manner than the claimed subject matter. No basis exists in Nason for the recited "acts of decrypting and re-encrypting taking place on a per cache page basis and being performed by encryption/decryption hardware integrated with the GPU". Nason *teaches away* from such features by relying upon a software driver, which is separate from the GPU and resides between the OS and Hardware.

Again, even if Nason is construed as providing a basis for "per cache page basis", this would occur in Nason via the SEDD which is consistently and clearly described as software residing "between the operating system device drivers 405 and the hardware". Accordingly, Nason fails to provide any basis for, and is in fact directly contrary to, "acts of decrypting and re-encrypting taking place on a per cache page basis and being performed by encryption/decryption hardware integrated with the GPU" as presently recited in claim 1. Accordingly, claim 1 is allowable for at least these reasons and withdrawal of the §103 rejection is respectfully requested.

Claims 2-11 depend from claim 1 and are allowable at least on the basis of this dependency as well as for their own recited features which the references of record fail to disclose, teach, or suggest. Accordingly, withdrawal of the rejections of claims 2-11 is respectfully requested.

Each of claims 12, 23, 31, 39, 45, 53, 70 and 87 has been amended to recite in varying terms and scope features similar to "at least one of said acts of decrypting and re-encrypting taking place on a per cache page basis and being performed by encryption/decryption hardware integrated with the GPU" as presently recited in claim 1.

Accordingly, claims 12, 23, 31, 39, 45, 53, 70 and 87 and their associated dependent claims are allowable over the references of record based on similar reasoning. Accordingly, withdrawal of the rejections of claims 12-94 is respectfully requested.

Conclusion

The Application is in condition for allowance and the Applicant respectfully requests reconsideration and issuance of the present application. Should any issue remain that prevents immediate issuance of the application, the Examiner is requested to contact the undersigned attorney to discuss the unresolved issue.

Respectfully submitted,

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